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EXAMINER	
LEE, CHUN KUAN	
ART UNIT	PAPER NUMBER
2181	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/31/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/750,013	SCHMIDT ET AL.	
	Examiner	Art Unit	
	Chun-Kuan (Mike) Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *08/02/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

RESPONSE TO ARGUMENTS

1. Applicant's arguments filed 08/18/2006 have been fully considered but they are not persuasive.

2. In responding to applicant's argument regarding the rejection of independent claims 1 and 6 rejected under 35 U.S.C. 103(a) that Sharma and Togawa are nonanalogous art, because Sharma is directed to preventing overflow and underflow across an asynchronous channel and Togawa is directed towards power control; further more, applicant argued that it would not have been obvious to combine Sharma and Togawa because Sharma is not concern with power consumption problems, as stated on page 9, last paragraph, to page 11, 2nd paragraph. Applicant's arguments have fully been considered, but are not found to be persuasive.

Sharma is directed towards asynchronous data transferring wherein the receiving and the transferring of data are operating at different clock frequencies (Sharma, Abstract and col. 3, ll. 64-67), and Togawa teaches the transferring of data between a CPU (Togawa, Fig. 5, ref. 101) and a display device (i.e. peripheral device) (Togawa, Fig. 5, ref. 113) via an interface circuit (Togawa, Fig. 5, ref. 145), wherein it is well known to one of ordinary skilled in the art that the CPU's operating clock frequency is different from the display device's operating clock frequency.

Further more, neither Sharma nor Togawa teaches that by combining with the other, the resulting combination would fail technologically, such that the combination will not work, and it would have been obvious to combine Sharma and Togawa for the benefit of further improving Sharma's regulation of asynchronous data transferring to include Togawa's regulation of power for Sharma's chip core logics enabling efficient power utilization for the chip corelogics.

3. In responding to applicant's argument regarding the independent claims 1 and 6 rejected under 35 U.S.C. 103(a) that the combined teaching of Sharma and Togawa fail to suggest "detecting a non-data sequence at an inlet of a buffer and passing an indicator that refers to such detection through the buffer," as stated on page 11, 3rd paragraph. Applicant's arguments have fully been considered, but are not found to be persuasive.

Please note that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

More specifically, applicant's arguments appear to be referencing that the claimed limitation "... to prevent overflow of the buffer, and in response to

(i) detecting the non-data sequence at an inlet of the buffer and

(ii) passing an indicator that refers to such detection through the buffer,

changing the unload pointer by more than one entry so that a non-data symbol of the non-data sequence, as loaded in the buffer, is skipped while unloading..." was not taught or suggest by the combined references of Sharma and Togawa. The examiner relied on the references as following for the rejection of the above claimed limitation.

Sharma teaches a buffer underflow and overflow prevention method and apparatus comprising preventing buffer (FIFO buffer 502 of Fig. 5) overflow, and in responding to detecting the non-data sequence (Fig. 7, ref. 712) at an inlet of the buffer, changing the unload pointer (read pointer 510 of Fig 5) by more than one entry so that a non-data symbol (e.g. drop me packet) of the non-data sequence, as loaded in the buffer, is skipped while unloading (e.g. reading) (Abstract; col. 6, ll. 6-12; col. 7, l. 67 to col. 8, l. 12 and col. 8, ll. 30-35).

Togawa teaches a system and a method comprising passing (e.g. passing by writing) an indicator (e.g. power save control information) to a register (e.g. buffer) resulted from the detection of the type of data (Fig. 8, ref. S 2-2) ([0111]-[0114]).

By combining Togawa's indicator information into Sharmau's flow and overflow prevention method and apparatus, the resulting combination of the references further teaches the buffer underflow and overflow prevention method and apparatus comprising wherein the detection of the type of data including drop me packet (i.e. the non-data sequence) is passed utilizing the indicator through the buffer for the prevention of buffer overflow.

4. In responding to applicant's argument regarding the independent claims 11, 15, 21, 24 and 28 rejected under 35 U.S.C. 103(a) that the combined references of Sharma and Togawa fail to teach/suggest every claimed limitations of independent claims 11, 15, 21, 24 and 28, because Sharma and Togawa are nonanalogous art, as Sharma is directed to preventing overflow and underflow across an asynchronous channel and Togawa is directed towards power control, as stated on pages 12-13. Applicant's arguments have fully been considered, but are not considered to be persuasive.

Please view the examiner's detailed response above in regards to Sharma and Togawa are analogous art.

5. In responding to applicant's argument regarding the independent claims 11, 15, 21, 24 and 28 rejected under 35 U.S.C. 103(a) that there is no motivation for combining Sharma and Togawa, as stated on pages 12-13. Applicant's arguments have fully been considered, but are not considered to be persuasive.

It would have been obvious to combine Sharma and Togawa for the benefit of further improving Sharma's regulation of asynchronous data transferring to include Togawa's regulation of power for Sharma's chip core logics enabling efficient power utilization for the chip corelogics.

6. As per claims 2-5, 7-10, 12-14, 16-20, 22-23, 25-27 and 29-33, dependent claims 2-5, 7-10, 12-14, 16-20, 22-23, 25-27 and 29-33 are unpatentable at least due to direct or indirect dependency on the rejected independent claims 1, 6, 11, 15, 21, 24 and 28.

7. In responding to all applicant's arguments, the examiner maintains his position and rejected the claims 1-33 in detail below.

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

8. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

II. INFORMATION CONCERNING DRAWINGS

Drawings

9. The applicant's drawings submitted are acceptable for examination purposes.

iii. ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

As required by **M.P.E.P. 609(C)**, the applicant's submissions of the Information Disclosure Statement dated August 02, 2007 is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P 609 C(2)**, a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

IV. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1-4, 6-9, 11-12, 14-16, 18, 20-21, 24-25, 27-29, 31 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sharma et al. (US Patent 6,813,275) in view of Togawa (US Patent 6,931,557).

12. As per claims 1 and 6, Sharma teaches a buffer underflow and overflow prevention method and apparatus comprising:

receiving a plurality of data in a receiver, the data having been transmitted by a transmitter and received over a serial point to point link that couples the receiver and the transmitter, wherein the plurality of data include a plurality of drop-me warning packets and a plurality of drop-me packets inserted according to a predetermined methodology into a data sequence by the transmitter (Abstract; Figure 3; Figures 6-7; column 4, line 58 to column 5, line 3 and column 7, lines 9-44, where "data" is read on "symbols", "receiver" is read on "first integrated circuit (IC) device", "transmitter" is read on "second IC device" "plurality of drop-me warning packets and a plurality of drop-me packets" is read on "non-data sequence");

writing the plurality of data into a synchronizing FIFO buffer according to a write pointer (Abstract; Figure 3 and column 4, lines 35-57, where "writing" is read on "loading" and "write pointer" is read on "load pointer");

reading the data sequence and some of the drop-me warning packets and the drop-me packets from the synchronizing FIFO buffer according to a reading pointer that points to different entries of the synchronizing FIFO buffer, wherein the reading pointer is changed by one entry each time a symbol is unloaded (Abstract; Figure 3 and column 5, line 42 to column 6, line 12, where "reading" is read on "unloading" and "reading pointer" is read on "changing unload pointer");

to prevent overflow of the synchronizing FIFO buffer, and in response to detecting the drop-me warning packets and drop-me packets at an inlet of the synchronizing FIFO buffer, changing the reading pointer by more than one entry so that the drop-me warning packets and the drop-me packets, as wrote in the buffer, is skipped while reading (Abstract; Figure 3; Figure 5 and column 5, line 42 to column 6, line 12); and

to prevent underflow of the buffer, and in response to detecting the drop-me warning packets and the drop-me packets at an inlet of the buffer stalling the reading pointer at an entry of the buffer that contains the drop-me packets while reading (Abstract; Figure 3; Figure 5 and column 5, line 42 to column 6, line 12).

Sharma does not teaches a buffer underflow and overflow prevention method and apparatus comprising passing an indicator that refers to the detection of non-data sequence through the buffer.

Togawa teaches an information processing method and apparatus comprising:

a CPU, wherein the CPU transmits data to a display deice (Figure 5, where "CPU" is read on "processor");

a memory (Figure 5, where "memory" is read on "main memory");

the graphic board controller that communicative couples the CPU to the display device (Figure 1 and Figure 5, where "graphic board controller" is read on "I/O controller hub" and "display device" is read on "peripheral device");

a gate which communicatively coupled to the CPU and the memory and provides the CPU with I/O access, the gate having a link interface circuitry (Figure 5, where "gate" is read on "integrated circuit (IC) device"); and

detecting the type of data to be transmitted and assigning a flag to said data in accordance to the type of data detected, wherein the flag is use by a controller for regulating the computer system (Figure 8 and column8, line 49 to column 9, line 50).

Therefore, it would have been obvious to one of ordinary skill in this art, at the time of invention was made to modify Sharma to include in the synchronizing FIFO buffer underflow and overflow prevention method and apparatus comprising passing a flag that refers to the detection of the drop-me warning packets and the drop-me packets through the synchronizing FIFO buffer.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to have modify Sharma by the teaching of Togawa, because to include in the buffer underflow and overflow prevention method and apparatus comprising passing a flag that refers to the detection of the drop-me warning packets

and the drop-me packets through the synchronizing FIFO buffer, would provide a more accurate flow control and also further improve the control to the computer system by including power control.

13. As per claim 2, Sharma as modified teaches a buffer underflow and overflow prevention method and apparatus where the non-data sequence is detected by detecting a combination of the drop-me warning packets follow by the drop-me packets, different non-data symbol in said non-data sequence (Sharma, column 5, lines 42-57, where "drop-me warning packets" is read on "first non-data symbol" and "drop-me packets" is read on "second non-data symbol").

14. As per claims 3, 11, 15, 20-21, 24 and 28, Sharma teaches a buffer underflow and overflow prevention method and apparatus comprising:

a transmitter chip core logic and a receiving chip core logic (Abstract and Figure 3);

interface logic between the transmitter and the receiver, wherein the interface logic receive data from the transmitter and output the data to the receiver serially, comprising of the synchronizing FIFO buffer to regulate data between the transmitter and the receiver (Abstract; Figure 3; column 4, lines 35-57 and column 5, line 58 to column 6, line 12);

the synchronizing FIFO buffer having an input to receive a plurality of data that were transmitted by the transmitter over a serial point-to-point data link, the buffer

having a plurality of entries (Abstract; Figure 3, where "FIFO buffer" is read on "buffer", "data" is read on "symbols" and "data link" is read on "link");

write pointer circuitry to provide a write pointer to write the plurality of data into the plurality of entries of the synchronizing FIFO buffer, respectively (Abstract; Figures 3-5; column 5, lines 4-32, where "write pointer circuitry" is read on "first pointer logic", "write pointer" is read on "first pointer" and "write" is read on "load");

read pointer circuitry to provide read pointer to sequentially read the plurality of data from the plurality of entries of the synchronizing FIFO buffer, respectively (Abstract; Figures 3-5; column 5, lines 4-32, where "read pointer circuitry" is read on "second pointer logic", "read pointer" is read on "read pointer" and "read" is read on "unload");

subtractor comparing the read and write pointers (Abstract; Figures 3-5; column 5, lines 4-32, where "subtractor" is read on "comparison logic");

pointer control logic having an output coupled to the read pointer circuitry,

wherein the pointer control logic is to stall the read pointer at an entry that contains a plurality of drop-me warning packets and a plurality of drop-me packets, in response to a) detecting the drop-me warning packets and the drop-me packets at the output of the FIFO buffer, and b) the subtractor indicating the buffer is less full than an ideal number of entries (Abstract; Figures 3; Figure 5 and column 5, line 58 to column 6, line 12, where "a plurality of drop-me warning packets and a plurality of drop-me packets" is read on "identifier" and "ideal number of entries" is read on "predetermined threshold"); and

wherein he pointer control logic is to advance the read pointer by more than one entry to skip over an entry that contain the drop-me packet, in response to a) detecting the plurality of drop-me warning packets and the plurality of drop-me packets at the output of the FIFO buffer, and b) the subtractor indicating the buffer is more full than an ideal number of entries (Abstract; Figures 3; Figure 5 and column 5, line 58 to column 6, line 12, where "drop-me packets" is read on "non-data symbol").

Sharma does not teach a buffer underflow and overflow prevention method and apparatus comprising:

a processor;

a main memory;

a integrated circuit (IC) device which communicatively coupled to the processor and the main memory and provides the processor with I/O access, the IC device having a link interface circuitry that supports a serial, point to point link, the circuitry includes:

detection logic having an input to receive a plurality of symbols and an output to feed the input of the buffer a non-data symbol sequence identifier;

generating a flag in response to the detecting of the first and second non-data symbols of said non-data sequence, and aligning the flag with the first non-data symbol when loading the flag with said non-data sequence into the buffer; and

the interface unit is an I/O controller hub that communicatively couples the processor to peripheral device.

Togawa teaches an information processing method and apparatus comprising:

a CPU, wherein the CPU transmits data to a display deice (Figure 5);

a memory (Figure 5);

the graphic board controller that communicative couples the CPU to the display device (Figure 1 and Figure 5);

a gate which communicatively coupled to the CPU and the memory and provides the CPU with I/O access, the gate having a link interface circuitry (Figure 5); and

detecting the type of data to be transmitted and assigning a flag to said data in accordance to the type of data detected, wherein the flag is use by a controller for regulating the computer system (Figure 8 and column8, line 49 to column 9, line 50).

Therefore, it would have been obvious to one of ordinary skill in this art, at the time of invention was made to modify Sharma to include in the buffer underflow and overflow prevention method and apparatus comprising:

a CPU;

a memory;

detection logic having an input to received the plurality of data from the CPU,

an output to feed the input of the synchronizing FIFO buffer,

detecting the type of data to at an inlet of the synchronizing FIFO buffer, and

assigning a flag indicating the type of data detected for the purpose of regulating the data flow, comprising assigning and aligning the flag to the drop-me warning packets when writing the drop-me warning packets into the synchronizing FIFO buffer (where "predefined non-data symbol sequence" and "synchronizing FIFO buffer" is read on "elastic buffer", "assigning a flag" is read on "passing an indicator");

detecting the assigned flag associated with the drop-me warning packet at an outlet of the synchronizing FIFO buffer to avoid one of the overflow and underflow conditions in the synchronizing FIFO buffer; and

the interface logic communicatively couples the CPU to the display device.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to have modify Sharma by the teaching of Togawa, because to include in the buffer underflow and overflow prevention method and apparatus comprising:

a CPU;

a memory; and

detection logic having an input to received the plurality of data from the CPU,

an output to feed the input of the synchronizing FIFO buffer,

detecting the type of data to at an inlet of the synchronizing FIFO buffer, and

assigning a flag indicating the type of data detected for the purpose of regulating the data flow, comprising assigning and aligning the flag to the drop-me warning packets when writing the drop-me warning packets into the synchronizing FIFO buffer; and

detecting the assigned flag associated with the drop-me warning packet at an outlet of the synchronizing FIFO buffer to avoid one of the overflow and underflow conditions in the synchronizing FIFO buffer; and

the interface logic communicatively couples the CPU to the display device would allow further improvement to the overall control of the computer system and further include the power control of the peripheral coupled to the CPU.

15. As per claim 4, Sharma as modified teaches a buffer underflow and overflow prevention method and apparatus comprising wherein the read pointer is changed or stalled in response to detecting the flag associated to the drop-me warning packet at an output of the FIFO buffer, so that the drop-me packet, as wrote in the FIFO buffer, is skipped or the reading is stalled (Sharma, Abstract; Figures 3-5 and column 5, line 42 to column 6, line 12).

16. As per claim 12, Sharma as modified teaches a buffer underflow and overflow prevention method and apparatus comprising wherein the plurality of data are to be received in accordance with the a first clock signal which can be derived by the interface logic from the clock transmitted by the transmitter (Sharma, Abstract; Figures 3-5; column 4, line 58 to column 5, line 32, where "clock transmitted by the transmitter" is read on "transmit clock from another IC device").

17. As per claim 14, Sharma as modified teaches a buffer underflow and overflow prevention method and apparatus comprising wherein the read pointer circuitry is to advance the read pointer in accordance with a second clock signal that is derived from the receiver clock of the receiving chip clock domain,

and wherein the write pointer circuitry is to advance the write pointer according with the first clock signal (Sharma, Abstract and Figures 3-5, where "receiver clock of the receiving chip clock domain" is read on "local clock of the root complex").

18. Claims 7-9, 16, 18, 25, 27, 29, 31 and 33 repeat the limitations of claims 2-4, 12 and 14 and are therefore rejected accordingly.

19. Claims 5 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sharma et al. (US Patent 6,813,275) in view of Tseng et al. (US Patent 6,678,756), further in view of the "PCI-Express: The upcoming Standard" and further in view of the "PCI Express Base Specification Revision 1.0a".

As per claim 5 and 10, Sharma does not teaches a buffer underflow and overflow prevention method and apparatus comprising wherein the bus interconnecting the transmitter and the receiver is a PCI bus.

Tseng teaches a control system and method for a FIFO buffer comprising the PCI bus coupled to the CPU and the memory in a computer system (Figure 1 and column1, lines 12-43); and

an interface logic comprising of FIFO array and FIFO controller coupling the PCI interface to the memory (Figure 6).

Therefore, it would have been obvious to one of ordinary skill in this art, at the time of invention was made to modify Sharma to include in the buffer underflow and

overflow prevention method and apparatus comprising wherein the bus interconnecting the transmitter and the receiver is a PCI bus in a computer system.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to have modify Sharma by the teaching of Tseng, because to include in the buffer underflow and overflow prevention method and apparatus comprising wherein the bus interconnecting the transmitter and the receiver is a PCI bus in a computer system, because not only is the PCI bus one of the most well know type of bus to one skilled in the art, Togawa's FIFO control system and method is programmable instead of being fixed therefore will provide a more efficient bandwidth utilization of the PCI bus.

Sharma as modified does not teaches a buffer underflow and overflow prevention method and apparatus comprising wherein the PCI bus is a PCI Express bus.

The "PCI-Express: The upcoming Standard" teaches the utilization of PCI express bus in a computer system, wherein the PCI Express is coupled to the memory and the CPU (Please see figure on page 1 and paragraphs 1-3 on pages 1-2)

Therefore, it would have been obvious to one of ordinary skill in this art, at the time of invention was made to modify Sharma as modified by Tseng to include in the buffer underflow and overflow prevention method and apparatus comprising wherein the bus interconnecting the transmitter and the receiver is a PCI Express bus in a computer system.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to have modify Sharma as modified by Tseng with the teaching of the "PCI-Express: The upcoming Standard", because to include in the buffer underflow and overflow prevention method and apparatus comprising wherein the bus interconnecting the transmitter and the receiver is a PCI Express bus in a computer system, would provide high-bandwidth interconnection with low pin-count as well as low-overhead and low latency data transfers to maximizing interconnect efficiency.

Sharma as modified does not teaches a buffer underflow and overflow prevention method and apparatus comprising non-data sequence including the symbol COM and the symbol SKP transmitted over the PCI Express bus.

The "PCI Express Base Specification Revision 1.0a" teaches the transmission of the symbol COM for initialization following by the symbol SKP (Section 4.2.1.2. pages 153-154).

Therefore, it would have been obvious to one of ordinary skill in this art, at the time of invention was made to modify Sharma as modified Tseng and the "PCI-Express: The upcoming Standard" by including in the buffer underflow and overflow prevention method and apparatus comprising the PCI Express bus, wherein non-data sequence conforms to PCI Express standard and therefore includes the symbol COM followed by the symbol SKP.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to have modify Sharma as modified Tseng and the "PCI-Express:

The upcoming Standard" by the teaching of the "PCI Express Base Specification Revision 1.0a", because to include in the buffer underflow and overflow prevention method and apparatus comprising the PCI Express bus, wherein non-data sequence conforms to PCI Express standard and therefore includes the symbol COM followed by the symbol SKP, would be necessary as the system conforms to the PCI Express standard and thus provide proper symbol encoding for the data transmission on the PCI bus.

20. Claims 13, 17, 26 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sharma et al. (US Patent 6,813,275) in view of Togawa (US Patent 6,931,557) as applied to claim 1-4, 6-9, 11-12, 14-16, 18, 20-21, 24-25, 27-29, 31 and 33 above, and further in view of Okawa et al. (US Pub.: 2002/0010824).

As per claim 13, Sharma as modified does not teaches a buffer underflow and overflow prevention method and apparatus comprising wherein the first clock signal is to be derived from the transmit clock being embedded in a stream of information that contains the plurality of symbols and is to be transmitted by said another IC device.

Okawa teaches a serial data transmission system and method comprising Data/Strobe link encoding method, wherein the transmitter clock is embedded in the stream of data transmitted (Figure 1 and [0004] on page 1).

Therefore, it would have been obvious to one of ordinary skill in this art, at the time of invention was made to modify Sharma as modified by Togawa to include in the buffer underflow and overflow prevention method and apparatus comprising wherein the

first clock signal is to be derived from the transmitter clock being embedded in a stream of information that contains the plurality of data and is to be transmitted by the transmitter.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to have modify Sharma as modified by Togawa by the teaching of Okawa, because to include in the buffer underflow and overflow prevention method and apparatus comprising wherein the first clock signal is to be derived from the transmitter clock being embedded in the stream of information that contains the plurality of data and is to be transmitted by the transmitter, would enable better accuracy of deriving the high frequency transmitter clock from the data by transmitting and utilizing a strobe signal that have a lower frequency than the transmitter clock.

21. Claims 17, 26 and 30 repeat the limitations of claim 13 and are therefore rejected accordingly.

22. Claim 19, 23 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sharma et al. (US Patent 6,813,275) in view of Togawa (US Patent 6,931,557) as applied to claim 1-4, 6-9, 11-12, 14-16, 18, 20-21, 24-25, 27-29, 31 and 33 above, and further in view of Tseng et al. (US Patent 6,678,756).

As per claim 19 and 23, Sharma as modified teach the buffer underflow and overflow prevention method and apparatus comprising:

the FIFO buffer (Sharma, Figure 3);

the interface logic communicatively couples the CPU, the memory and the display device (Togawa, Figure 1, where "display device" is read on "graphics element").

Sharma as modified does not teach the buffer underflow and overflow prevention method and apparatus comprising wherein the processing is desired to maintain the elastic buffer in a half-full state; and

the interface unit communicatively coupled the processor to the main memory and the graphics element.

Tseng teaches a control system and method for a FIFO buffer comprising of setting the half-full flag (column 5, line 61 to column 6, line 6 and column 7, lines 31-41);

North Bridge communicative coupling the CPU to the memory and the PCI interface (Figure 1); and

an interface logic comprising of FIFO array and FIFO controller coupling the PCI interface to the memory (Figure 6, where "interface unit" is read on "memory controller hub").

Therefore, it would have been obvious to one of ordinary skill in this art, at the time of invention was made to modify Sharma as modified by Togawa to include in the buffer underflow and overflow prevention method and apparatus comprising:

wherein the processing is designed to maintain the FIFO buffer in a half-full state; and

the interface unit communicatively couples the CPU to the memory and the display device.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to have modify Sharma as modified by Togawa by the teaching of Tseng, because to include in the buffer underflow and overflow prevention method and apparatus comprising:

wherein the processing is designed to maintain the FIFO buffer in a half-full state; and

the interface unit communicatively couples the CPU to the memory and the display device, would allow more efficient utilization of the FIFO buffer especially since Togawa's FIFO control system and method is programmable instead of being fixed.

23. Claim 32 repeats the limitations of claim 19 and is therefore rejected accordingly.

24. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sharma et al. (US Patent 6,813,275) in view of Togawa (US Patent 6,931,557) as applied to claim 1-4, 6-9, 11-12, 14-16, 18, 20-21, 24-25, 27-29, 31 and 33 above, and further in view of Tseng et al. (US Patent 6,678,756), the "PCI-Express: The upcoming Standard" and the "PCI Express Base Specification Revision 1.0a".

As per claim 22, Sharma as modified does not teaches a buffer underflow and overflow prevention method and apparatus comprising wherein the bus interconnecting the transmitter and the receiver is a PCI bus.

Tseng teaches a control system and method for a FIFO buffer comprising the PCI bus coupled to the CPU and the memory in a computer system (Figure 1 and column1, lines 12-43); and

an interface logic comprising of FIFO array and FIFO controller coupling the PCI interface to the memory (Figure 6).

Therefore, it would have been obvious to one of ordinary skill in this art, at the time of invention was made to modify Sharma as modified by Togawa to include in the buffer underflow and overflow prevention method and apparatus comprising wherein the bus interconnecting the transmitter and the receiver is a PCI bus in a computer system.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to have modify Sharma as modified by Togawa with the teaching of Tseng, because to include in the buffer underflow and overflow prevention method and apparatus comprising wherein the bus interconnecting the transmitter and the receiver is a PCI bus in a computer system, because not only is PCI bus one of the most well know type of bus to one skilled in the art, Togawa's FIFO control system and method is programmable instead of being fixed therefore will provide a more efficient bandwidth utilization of the PCI bus.

Sharma as modified does not teaches a buffer underflow and overflow prevention method and apparatus comprising wherein the PCI bus is a PCI Express bus.

The "PCI-Express: The upcoming Standard" teaches the utilization of PCI express bus in a computer system, wherein the PCI Express is coupled to the memory and the CPU (Please see figure on page 1 and paragraphs 1-3 on pages 1-2)

Therefore, it would have been obvious to one of ordinary skill in this art, at the time of invention was made to modify Sharma as modified by Togawa and Tseng to include in the buffer underflow and overflow prevention method and apparatus comprising wherein the bus interconnecting the transmitter and the receiver is a PCI Express bus in a computer system.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to have modify Sharma as modified by Togawa and Tseng with the teaching of the "PCI-Express: The upcoming Standard", because to include in the buffer underflow and overflow prevention method and apparatus comprising wherein the bus interconnecting the transmitter and the receiver is a PCI Express bus in a computer system, would provide high-bandwidth interconnection with low pin-count as well as low-overhead and low latency data transfers to maximizing interconnect efficiency.

Sharma as modified does not teaches a buffer underflow and overflow prevention method and apparatus comprising non-data sequence including the symbol COM and the symbol SKP transmitted over the PCI Express bus.

The "PCI Express Base Specification Revision 1.0a" teaches the transmission of the symbol COM for initialization following by the symbol SKP (Section 4.2.1.2. pages 153-154).

Therefore, it would have been obvious to one of ordinary skill in this art, at the time of invention was made to modify Sharma as modified by Togawa, Tseng and the "PCI-Express: The upcoming Standard" by including in the buffer underflow and overflow prevention method and apparatus comprising the PCI Express bus, wherein non-data sequence conforms to PCI Express standard and therefore includes the symbol COM followed by the symbol SKP.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to have modify Sharma as modified by Togawa, Tseng and the "PCI-Express: The upcoming Standard" by the teaching of the "PCI Express Base Specification Revision 1.0a", because to include in the buffer underflow and overflow prevention method and apparatus comprising the PCI Express bus, wherein non-data sequence conforms to PCI Express standard and therefore includes the symbol COM followed by the symbol SKP, would be necessary as the system conforms to the PCI Express standard and thus provide proper symbol encoding for the data transmission.

V. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1-33 have received a **FINAL ACTION** on the merits. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

IMPORTANT NOTE

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

January 24, 2007

Chun-Kuan (Mike) Lee
Examiner
Art Unit 2181

DONALD SPARKS
SUPERVISORY PATENT EXAMINER